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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,015	02/16/2001	Frank Nico Lieven Op'T Eynde	Q62388	1583

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/784,015	Applicant(s) OP'T EYNDE ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspond nc addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1,2 and 4-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 and 15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 5 12-15 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikata et al (US Pat. 5786738).

Regarding claim 1, Ikata et al disclose a packaged integrated circuit (PIC) comprising:

- a radio communication/radio frequency(RF) filter chip component/IC die/module (33a/33b in Fig. 2A and 2B), the die being directly connected by bonding wires (34 in Fig. 2B) to a high frequency/RF antenna (RFA- 37a-c/36c in Fig. 2A) and respective terminals/wiring

- the IC die being included in the PIC, wherein

- the RFA comprises a portion of the PIC and being excluded from the IC die or being on the exterior surface of the IPC

(Fig. 2A, 2B and 5; Col. 5, line 1- Col. 6, line 27; Col. 2-11).

Regarding claim 2, Ikata et al further disclose the PIC which houses the RF component and the RFA comprising terminals and metal object/wiring patterns made of metals such as tungsten, copper, etc (Col. 6, line 57; Col. 7, line 5).

Regarding claim 5, Ikata et al further disclose the RFA comprising planar metal patterns (37 a, b, c, etc. in Fig. 2A) being separated from the ground/shield metal planes (GND planes in Fig. 2B) by insulating ceramic layers (32-1, 32-2, etc. in Fig. 2B; Col. 5 and 6).

Regarding claim 12, Ikata et al disclose the PIC being a RF module/ceramic package.

Regarding claim 13, as explained above for claim 1, Ikata et al further disclose the PIC/module comprising:

- the IC die being directly connected by bonding wires/metal wiring/wiring pattern including through holes/vias (see vias in Fig. 2B- not numerically referenced; Col. 5, line 2-36), and

- the wiring being routed through the electrical ground/shield patterns/planes (GND planes in Fig. 2B) interposed between the die and RFA.

Regarding claim 14, as explained above for claim 2, Ikata et al disclose the RFA comprising the metal.

Regarding claim 15, as explained above for claim 2, Ikata et al disclose the RFA comprising the planar metal patterns being separated from the ground/shield metal planes by insulating ceramic layers.

Regarding claim 26, as explained above for claim 13, Ikata et al disclose the wiring comprising electrical ground/shield patterns/planes.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Masahito (Japanese Pat. 08250913, IDS paper #3).

Regarding claim 4, Ikata et al fail to specify the RFA being disposed on a metal frame.

Masahito teaches forming/disposing a RFA on a conventional metal lead frame/terminal (203 in Fig. 13; Detailed Description pp. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to dispose a RFA on a metal frame configuration so that a range of external connection capabilities can be achieved using Masahito's structure in Ikata's PIC.

5. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Koichi (Japanese Pat. 63181505, IDS paper #3) and Yoshikata (Japanese Pat. 06085530, IDS paper #3).

Regarding claim 6, Ikata et al further disclose forming maze-shape metal patterns by etching (Col. 6, line 3) but fail to specify the metal pattern being a metal slot pattern

Koichi (Fig. 2; pp. 1-4) and Yoshitaka (Fig. 1; pp. 1-6) teach forming a RFA having slot patterns including S-shaped slot and strip-line configuration respectively with predetermined dimensions to achieve the desired resonance frequency/impedance characteristics.

Furthermore, selecting the parameters and configuration of wiring such as shape/size, number of layers, pattern/layout on each layer, wire thickness/length, etc. in a high frequency/RF chip packaging and interconnection technology art is a subject

of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and signal propagation/performance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a RFA using a metal slot pattern consisting of a first S-shaped slot or a first slot and a second S-shaped slot which is rotated 90 degrees with respect to the first one so that the desired resonance frequency/impedance characteristics can be achieved and the transmission signal can be improved using Koichi and Yoshitaka's RFA design in Ikata's PIC.

Regarding claim 7, as explained above for claims 5 and 6, Ikata et al in view of Koichi and Yoshitaka teach using the slot pattern comprising a first S-shaped slot.

Regarding claim 8, as explained above for claims 5-7, Ikata et al in view of Koichi and Yoshitaka teach using a second S-shaped slot which is rotated 90 degrees with respect to the first one.

Regarding claim 16, as explained above for claims 13 and 6, Ikata et al in view of Koichi and Yoshitaka teach using the metal pattern being a metal slot pattern.

Regarding claim 17, as explained above for claims 13 and 7, Ikata et al in view of Koichi and Yoshitaka teach using the slot pattern comprising a first S-shaped slot.

Regarding claim 18, as explained above for claims 13 and 8, Ikata et al in view of Koichi and Yoshitaka teach using a second S-shaped slot which is rotated 90 degrees with respect to the first one.

6. Claims 9-11 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Houghton et al (US Pat. 6282095).

Regarding claim 9, Ikata et al fail to specify the PIC being a ball grid array (BGA).

Houghton et al teach using conventional packaging technologies such as a BGA, Small Outline Package (SOP), peripheral Quad Flat Pack (QFP), etc. in a RF module (Col. 5, line 15-25).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PIC being a ball grid array (BGA) so that a wide range of external connection capabilities can be configured using Houghton et al's structures in Ikata's PIC.

Regarding claim 10, as explained above for claim 9, Ikata et al in view of Houghton et al teach using the IPC being a QFP.

Regarding claim 11, as explained above for claim 9, Ikata et al in view of Houghton et al teach using the IPC being a SOP.

Regarding claim 23, as explained above for claim 9, Ikata et al in view of Houghton et al teach using the IPC being a QFP.

Regarding claim 24, as explained above for claim 10, Ikata et al in view of Houghton et al teach using the IPC being a QFP.

Regarding claim 25, as explained above for claim 11, Ikata et al in view of Houghton et al teach using the IPC being a SOP.

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Takeshi (Japanese Pat. 09237867, IDS paper #3).

Regarding claim 19, Ikata et al disclose the through holes/vias connecting the plurality of layers (32-1 through 32-4; Col. 5, line 18) in the PIC but fail to show an arrangement of the plurality of vias around the periphery of the RFA.

Takeshi discloses the RFA/package comprising conventional arrangement of a vias (14, 15, etc. in Fig. 3 and 1) around the periphery of the RFA.

Furthermore, selecting the parameters of wiring such as via size, number, location/pattern, wire thickness/length, etc. in a high frequency/high power chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and the module performance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select an arrangement of the plurality of vias being around the periphery or having two vias being opposite each other so that signal propagation, routing and performance can be improved using Takeshi's patterns in Ikata-et-al's-PIC.

Regarding claim 20, as explained above for claim 19, Ikata et al in view of Takeshi and Houghton et al teach selecting an arrangement having two vias being opposite each other.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Masahito (Japanese Pat. 08250913, IDS paper #3).

Regarding claim 21, as explained above for claim 13, Ikata et al disclose hermetically sealing the PIC but fail to specify encapsulating the package.

Moskowitz et al teaches using conventional encapsulation/resin sealing for a RF package (Fig. 1A/1B; Col. 2) to provide added protection.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to encapsulate the package sealing the die and the shield so that the desired sealing for the internal components can be provided using Moskowitz et al's sealing in Ikata's PIC.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Masahito (Japanese Pat. 08250913, IDS paper #3) and Moskowitz et al (US Pat. 5528222).

Regarding claim 22, as explained above for claims 4 and 21, Ikata et al in view of Masahito and Moskowitz et al teach disposing a RFA on a metal frame of the IPC.

10. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) in view of Sholley et al (US Pat. 6265774).

Regarding claim 27, Ikata et al fail to specify the length of the wire being 1/4 to ½ the wavelength of a transmitted or received radio signal.

Sholley et al teach using small dimensions for leads/wires serving as a full or one-half of the wavelength of high frequency antenna (Col. 1, line 25-55). Furthermore, determination of parameters and configuration of wiring such as wire thickness/length, pattern/layout of wiring layer, etc. with respect to the wavelength of transmitted signals in a high frequency/RF chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and signal propagation/performance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the length of the wire being 1/4 to ½ the wavelength of a transmitted or received radio signal so that signal propagation and performance can be improved using Sholley et al's wiring design in Ikata et al's PIC.

Response to Arguments

10. Applicant's arguments with respect to claims 1, 2 and 4-27 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-25-03

Tom Thomas

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